Verilog Simulation of Multichannel NAND Flash Memory

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Abstract— The storage system based on flash has very high demand than magnetic disk drives. Basically flash is a Non-Volatile memory in which the memory can be erased and programmed electrically. Flash memory consumes less power and latency compared to magnetic disk drives which makes flash more attractive and popular. Flash memory consists of Read, Write and Erase operations. In flash memory writing is done in pages and erasing in blocks. The parallel controller functions as a multichannel controller which is validated in accordance to the workloads that are spread.In this paper we explain about the design of new flash controller and also the required control signals for flash operations where parallelism is exploited by use of multiple channels or multiple controllers for a single flash which reduces latency for read, write and erase operations.

Index Terms— NAND Flash Controller; Multichannel; SSD;

1 Introduction

The increase in use of digital equipment's in present day scenario has led to improvements in memory modules. In previous days the basic memory is nothing but Magnetic disk drives. The severe drawback of magnetic disk drives is due to its mechanical system, high latency and more power consumption.Flash memory overcomes this drawback by having less latency, less power consumption and no mechanical system. Flash memory is faster than the traditional magnetic disk drives.There is mainly two types of flash memories available in the market, they are NAND flash memory and NOR flash memory. Basically this difference is because of the interconnection. Random access capability is high in NOR flash memory whereas NAND flash memory is famous for large density and high speed of read and write operations. NAND flash is used for large data storage.The flash memory used for large data storage is NAND flash. NAND flash is non-volatile and will be used mostly in day today's electronic and digital equipments. In solid state drivers (SSD's) NAND flash is one of the popular storage technology due to low power consumption, light weight and Non-volatility. NAND flash cell are made up of floating gate transistors. The threshold voltage of the floating gate transistors is programmed by injecting certain amounts of charge. The bit errors and bad blocks are handled by NAND controller and also maintains the high data accessing speed. Enhancing of reliability and increase of flash cycles in the flash memory is done by the flash controller is done by the flash controller. By incorporating an excellent NAND flash controller the system performance and product lifetime is improved. The designed NAND flash controller manages the flash memory chip efficiently by use of state machine. Further the paper is organized in following order. In second and third section motivation is described along with related works. In the fourth section, the architecture of multichannel NAND flash memory controller is explained. The results and conclusion is done in section 5 and 6.

2 Procedure for Paper Submission

Present day digital devices need a fast and powerful memory. Hard disk drives are very complex systems which consists of both electronic and mechanical components.teh major bottleneck for the system performance is due to low mechanical latency in many computing systems. The hard disk drives are also known for their high energy consumption which also effects complete device. Because of these drawbacks we moved to flash devices. Flash memory is improvised version of hard disk drives but their working complete differs from hard disk drives. Flash memory contains different logical sectors, where each logical sector contains many blocks and each block contains different pages and data will be stored in pages as shown in fig 1. Flash memory writes in pages and erases in blocks. Flash memories are very fast compared to previous hard disk drives and them well known for their less power consumption. The improved version of flash memory is multichannel flash memory. Where we use single flash memory but multiple controllers for the parallelism and to improve further latency.

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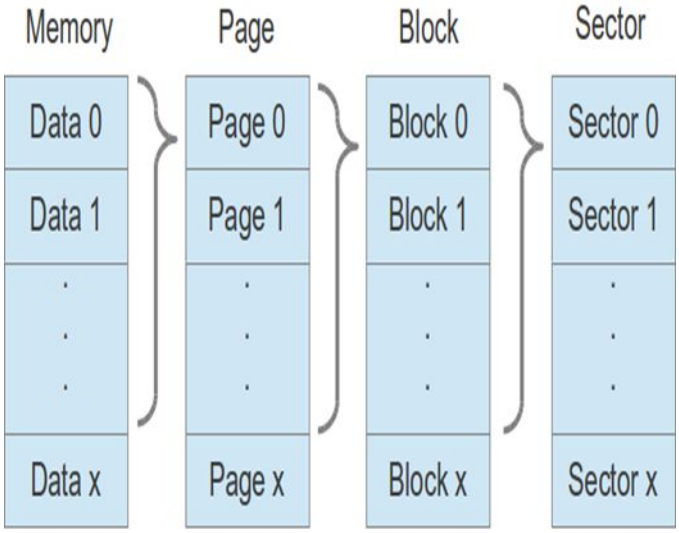

Fig .1.Flash memory Layout

3 RELATED WORK

In [3] Tang Li describes about basic controller design for flash memory. The controller basic work is to send the control signal or to measure the data adequacy. The proposed paper develop self designed controller to recognize and avoid mapping of invalid blocks.In [1] soya Teresa and Pradeep discuss about multichannel NAND Flash memory controller by using single controller for each and every channel. This paper basically exploits the parallelism of multiple channels in flash memory so that more than one instruction will be processed at a time so that the lot of latency will be reduced compare to single channel Flash memory controller.The paper [6] by koushal agrawal exploits use of Xilinx simulation for multi channel flash memory controller and it provide control signal in order to reduce the further complexity with respect to software simulation. Flash Translation layer plays very important role with respect to flash controller as it uses for logical and physical address mapping the paper [8] exploits about flash translation layer use in the controller design. The Scalable techniques for controller design have been shown in [4]. The controller designs with respect to SOC are shown in [5].

4 FLASH CONTROLLER

The following paper basically describes about the simulation done for the multichannel NAND flash memory over the XILINX platform. The multichannel is itself a miracle where it's been not a multi memory but it is a single memory with multiple controllers acting it as a multi-channel. Hence the controller architecture is much necessary for following paper work.The input to controllers are converted inputs from Flash Translation Layer (FTL). The host requests is translated into flash requests by FTL. In FTL host requests such as R/W is specified in terms of logical sectors. The channels of datapath and control signal are used by FTL to issue commands, address and data to the controller. The I/O controller takes both input and control signals. The both data will go to different set of register in order to access with flash memory. Different control signals are necessary in order to control this architecture hence we go for the special control signals which explained as below.

i) CE is high it shows that the controller is in working mode i.e., data is getting stored in memory when CE is low, the flash controller is not working.
ii) CLE: CLE indicates NAND flash clear. When CLE is high, data is cleared in main memory of controller. When CLE is low, no work takes place.
iii) ALE: ALE indicates NAND flash advanced latch enable. When ALE is high, it shows controller is working, when ALE is low, controller is in latch mode.
iv) WE: This indicates NAND flash in write operation. When WE is high, data writing process takes place which can be written to particular memory address. When WE is low, data cannot be written.
v) RE: This indicates NAND flash reset. When RE pin is low, working is proper when RE pin is high, the controller is set for reset mode and the entire operation of the flash controller will stop.

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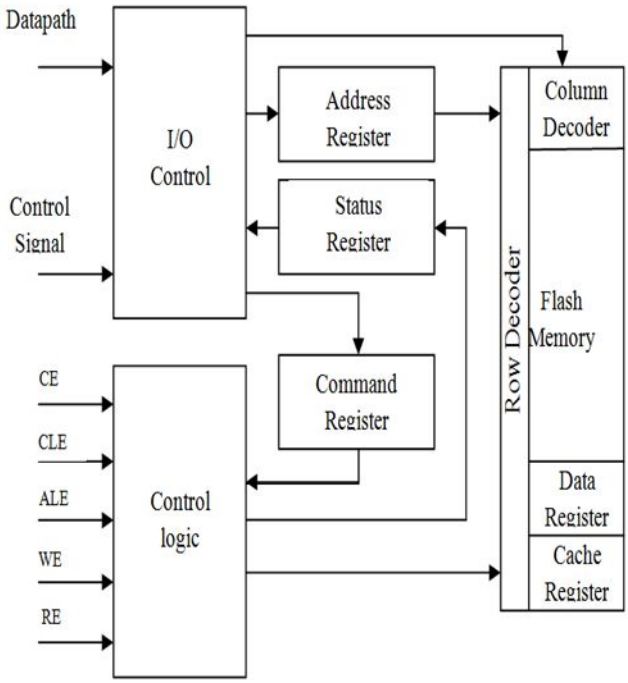

Fig 2. Block diagram of flash controller

5 MULTICHANNEL ARCHITECHTURE

Controller looks after the every instruction given to flash memory as the name indicates. Multichannel basically exploits parallelism in a flash memory. By using multiple controllers we achieve this parallelism. The basic multichannel flash design will be as shown in the figure 2.

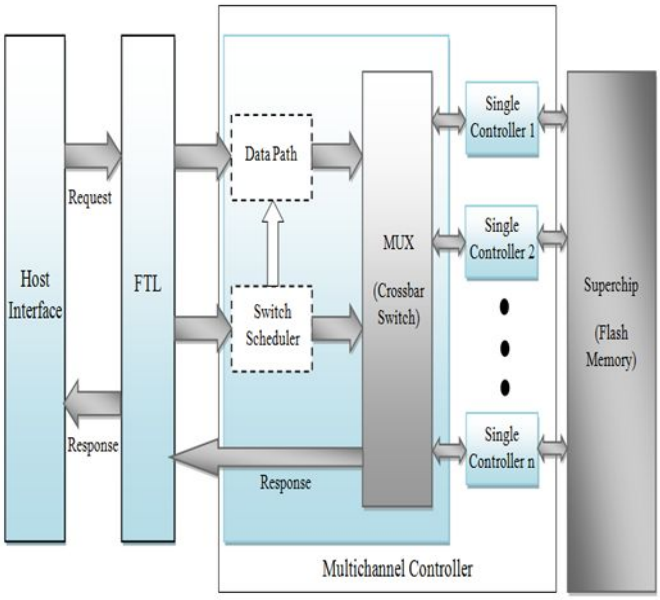

Fig 3. Multichannel NAND Flash design

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The host requests are directly fed into flash translation layer. This converts physical address to logical address. The multiplexer is used for the purpose of choosing the controller. The flash memory will be accessed through flash controller which chosen by mux. The logical address is converted into main logic and control logic. Main logic contains the data and control logic contains control signals for specific function to perform in controller such as write, read and erase.The control signal working can be seen by using finite state machine (FSM) as shown in fig 4.

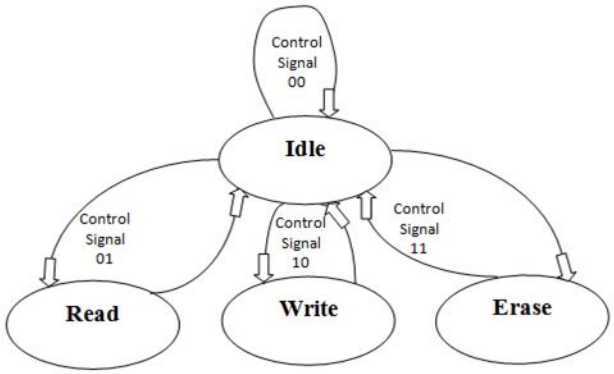

Fig .4. Finite state machine for controller.

The controller basically will be in idle state and they will move to read, write and erase state as shown in table 1. After completion of each function the controller will reach the ideal state.

TABLE 1
CONTROLLER OPERATIONS

Control signal	*Operation*	*Action*
00	Idle	Controller will be in idle state
01	Read	The data will be read by host from flash memory
10	Write	The data will be written into flash memory by host
11	Erase	The block of data will be erased from flash memory

6 RESULTS

With references to above discussion we simulated single and multi channel flash memory operations in order to see the various simulation results. Which are plotted as below, as shown in figures 5(a) to 5(f)

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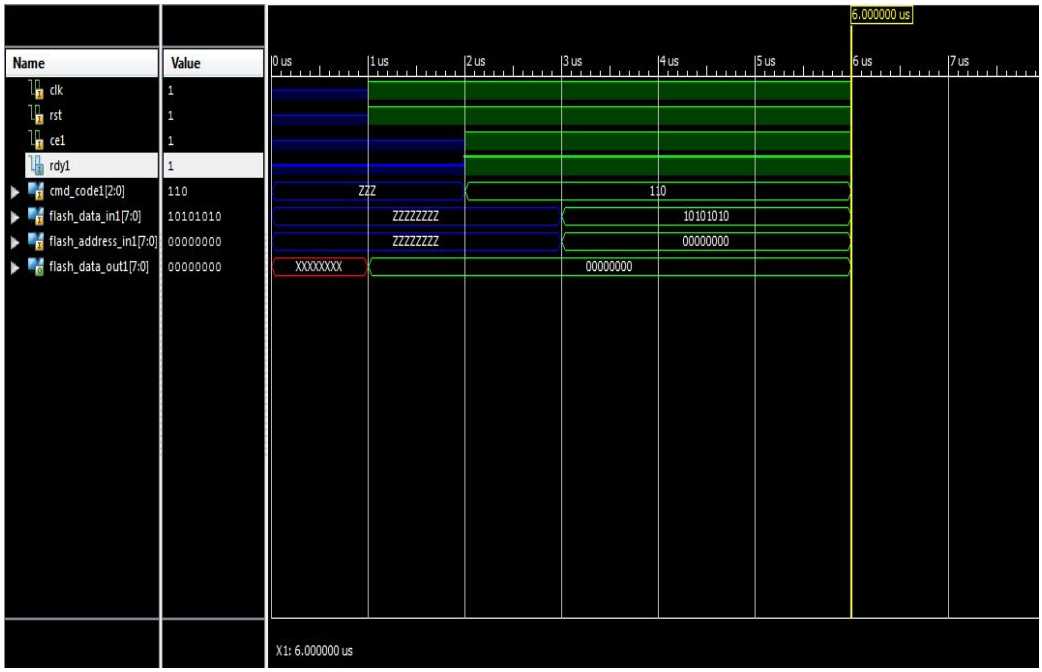

Fig .5(a).Single channel Write Operation

Fig .5(b).Single channel Read Operation

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Fig .5(c).Single channel Erase Operation

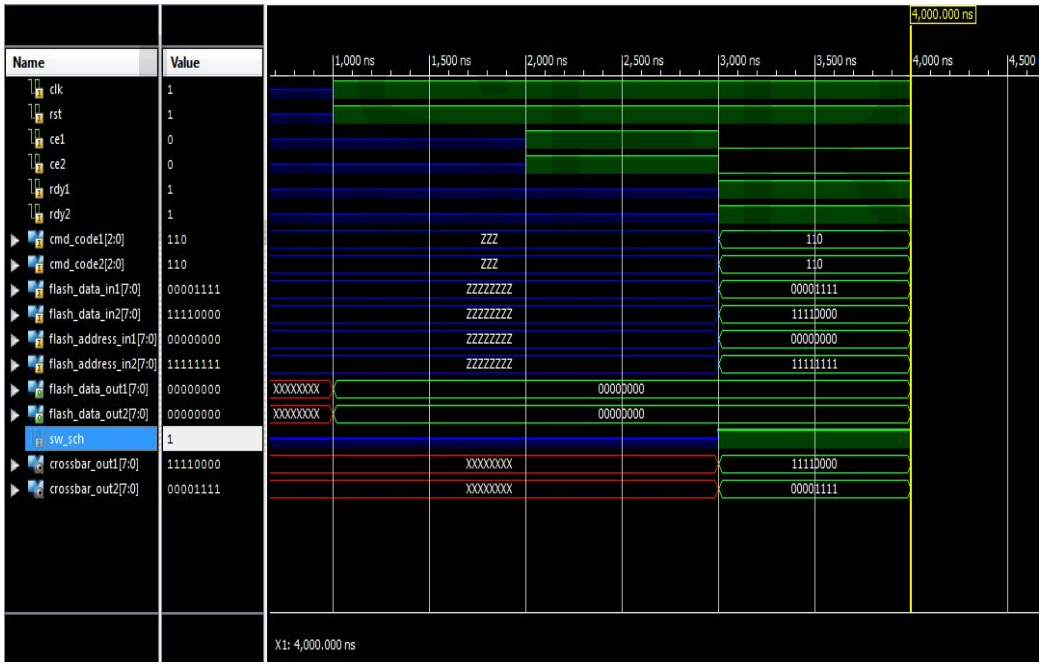

Fig 5(d). Multichannel Write Operation

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Fig .5(e) .Multichannel Read Operation

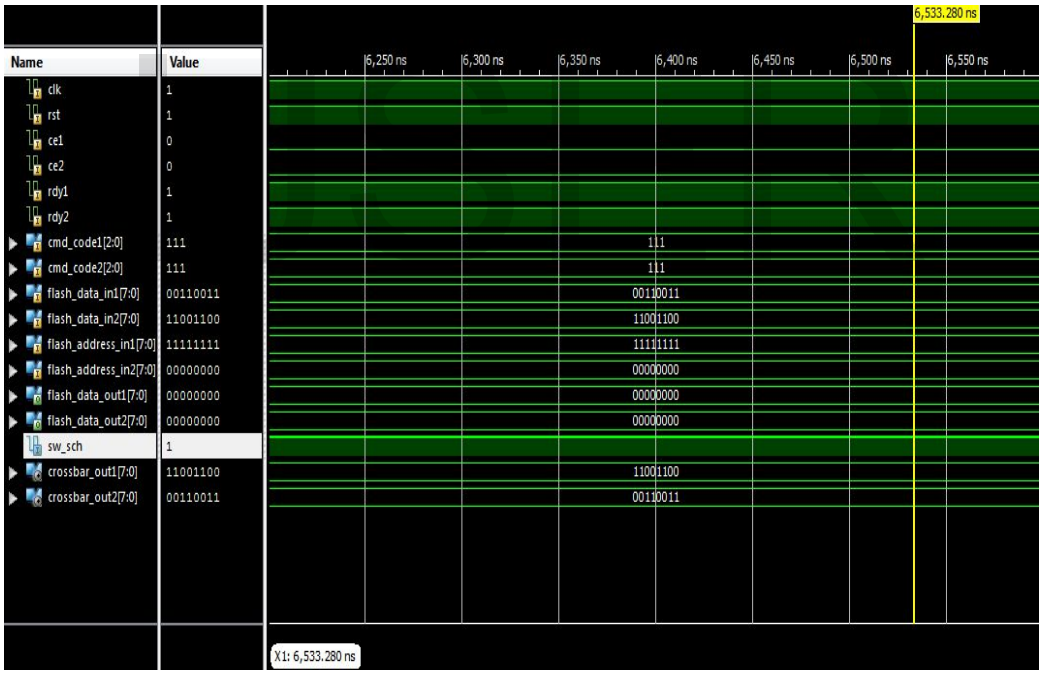

Fig .5(f). Multichannel Erase Operation

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7 CONCLUSION

The Controller for multichannel NAND Flash has been designed and parameters like latency and speed (IOPs) has been compared with HDD and single channel flash controller. It's been noticed that there will be great deduction in latency in multi-channel NAND Flash memory and also the input output request of multichannel is very high compared to single channel flash memory, hence they will be used in high data requesting devices.

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